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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/443,160	11/19/1999	DAVID L. ISAMAN	130.1012.02	6854

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/443,160	ISAMAN, DAVID L.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-21* is/are pending in the application.

4a) Of the above claim(s) *1* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,12-17,20 and 21* is/are rejected.

7)☒ Claim(s) *8-11,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. Attached
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2-21 remain for examination. Claims 1 has been canceled.

2. Upon further review and consideration, the finality of final office action on 06/01/04 has been withdrawn. The following is a non-final action.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pickett (5,854,921) in view of Amerson (5,475,823) .

3. As to claims 2,12, Pickett disclosed system including instructions which does not need address calculation to locate the operands (see col.2, lines 25-34). The operands were used to memory locations (see operand as memory location in col.8, lines 64-65). Pickett did not specifically show the detection of instructions as clamed. However Amerson disclosed a detection of instructions (see col.1, lines 30-41, col.4, lines 30-37, col.5, lines 16-19, see also the instruction detector in fig.5). It would have been obvious to one of ordinary skill in the art o use Amerson in Pickett for including the detection of the instruction without the calculations as clamed because the use of Amerson could provide the ability of Pickett o determine specific type of instruction

which required less cycle to process, therefore, increasing the flexibility of Pickett to adapt to different kind of instructions with a reduced time, and because Amerson did indicated the use of his instruction detection to reduce the instruction cycle (se col.), which would have been recognizable by one of ordinary skill in the art that the Amerson's instruction detection could be applicable into Pickett in order to determine the instructions with no address calculation and with the reduced cycle (see Pickett's desirability for including the instructions with reduced cycle in col2, lines 30-34), and for doing so, provided a motivation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-7, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson et al. (5,475,823) in view Srinivasan et al. (5,706,224) .

5. As to claims 2,12, Amerson disclosed a system for detecting an instruction (load) that loads data from a first memory location (A1) (see the loading of the memory address in col.l, lines 30-41, see co1.4, lines 30-37, co1.5, lines 16-19) that was previously stored to (e.g. see co1.8, lines 36-41).

6. Amerson et al. taught detection of a load that load data from memory location (e.g. see col.l , lines 30-41 , col.4, lines 30-37, col.5, lines 16-19) that was previously stored (see the store address accessed the same address as load , or previously by the store in col.8, lines 36- 43).

7. Amerson's address was referenced by load and store instructions (col.3, lines 1-10), the referenced address was shown to be the address (e.g. A3) of the load instruction (see col.2, lines 10). The referenced address (e.g. A3) was a value designated by the program as an address operand in the instruction , not by calculation. In other words, the address operand (e.g. A3) was a symbolic structure. This address specified by the load instruction was further taught to be compared to the address specified by other store instruction (e.g. see col.8, lines 29-42), and the subsequent action was that upon detection of the match, the data was forwarded to CPU (see col.8, lines 37-42).

8. Amerson is used based on the interpretation that Amerson did not specifically show the feature of without requiring computing the memory address as claimed. However, Srinivasan taught a system to locate a given data by means of comparison without having to know or compute the address or location of the information (see col.1, lines 59-67). It would have been obvious to one of ordinary skill in the art to use Srinivasan in Amerson for including the feature of without requiring the computation of the memory address as clamed because the use of Srinivasan could provide Amerson the ability to directly access the data needed for processing without the calculation for

the memory address , therefore, eliminating the extra read cycle from the memory, and Amerson did disclose a data forwarder (see col.8, lines 37-43) for forwarding the data upon detection of the same address specified by the load and store instructions (see col. e.g. see col.l , lines 60-65, col.2, lines 7-15, col.4, lines 43-48c01.6, lines 10-17, col.7, lines 20-26).), and the subsequent action was that the memory access was being bypassed (see the bypass path [data forwarder] in fig.5, see col.8, lines 37-43), therefore, providing a motivation to use the teaching of without having to calculate the address of the information in the memory by Srinivasan. Amerson is used as primary because it shows clearly the detection of the instruction (see fig.5, the instruction detector), and it showed clearly a memory location was previously stored (e.g. see the location was accessed by a store in col.8, lines 37-42. Srinivasan is used to supplement the explicit teaching of without calculation of address.

9. As to claims 3, 5, 13, 15, Amerson also detected store in a second location that was previously read (loaded, or read by load instruction. See detection of a store accessing the same address with a load in col.5, lines 29-38, col.6, lines 57-66).

10. As to claims 4,14, Amerson also included location previously stored (see col.8, lines 30-41).

11. As to claims 6,7,16,17, Amerson also included symbolic structure (see A3 in load instruction in col.2, line 10).

12. Claims 2-7, 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amerson et al. (5,475,823) in view Pickett (5,854,921) .

13. As to claims 2,12, Amerson disclosed a system for detecting an instruction (load that loads data from a first memory location (A1) (see the loading of the memory address in col.l, lines 30-41, see co1.4, lines 30-37, co1.5, lines 16-19) that was previously stored to (e.g. see co1.8, lines 36-41).

14. Amerson et al. taught detection of a load that load data from memory location (e.g. see col.l , lines 30-41 , col.4, lines 30-37, col.5, lines 16-19) that was previously stored (see the store address accessed the same address as load , or previously by the store in col.8, lines 36- 43).

15. Amerson's address was referenced by load and store instructions (col.3, lines 1-10), the referenced address was shown to be the address (e.g. A3) of the load instruction (see col.2, lines 10). The referenced address (e.g. A3) was a value designated by the program as an address operand in the instruction , not by calculation. In other words, the address operand (e.g. A3) was a symbolic structure. This address specified by the load instruction was further taught to be compared to the address specified by other store instruction (e.g. see col.8, lines 29-42), and the subsequent action was that upon detection of the match, the data was forwarded to CPU (see col.8, lines 37-42).

16. Amerson is used based on the interpretation that Amerson did not specifically show the feature of without requiring computing the memory address as claimed. However, Pickett disclosed a system including instructions without the need of

calculating the memory address (see col.2, lines 2-34). See also the address operand was directed to a memory location in col8, lines 64-65. It would have been obvious to one of ordinary skill in the art to use Pickett in Amerson for including the feature of without requiring the computation of the memory address as clamed because the use of Pickett could provide Amerson the ability to directly access the data needed for processing without the calculation for the memory address , therefore, avoiding delay time from accessing the memory, and Amerson did disclose a data forwarder (see col.8, lines 37-43) for forwarding the data upon detection of the same address specified by the load and store instructions (see col. e.g. see col.l , lines 60-65, col.2, lines 7-15, col.4, lines 43-48c01.6, lines 10-17, col.7, lines 20-26), and the subsequent action was that the memory access was being bypassed (see the bypass path [data forwarder] in fig.5, see col.8, lines 37-43, **see col.3, lines 31-40 for the data sent to the processor that would have been generated by the load instruction**), therefore, provided a motivation to use Pickett for not having to calculate the memory address.

17. As to claims 3, 5, 13, 15, Amerson also detected store in a second location that was previously read (loaded, or read by load instruction. See detection of a store accessing the same address with a load in col.5, lines 29-38, col.6, lines 57-66).

18. As to claims 4,14, Amerson also included location previously stored (see col.8, lines 30-41).

19. As to claims 6,7,16,17, Amerson also included symbolic structure (see A3 in load instruction in col.2, line 10).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. Claims 2-7, 12-17 are rejected under 35 U.S.C. 102 (b) as being anticipated by Amerson et al. (5,475,823) .

21. As to claims 2,12, Amerson is used based on the interpretation and a new argument that Amerson had implicit teaching of without calculation. Amerson included comparison of the load address with store address for determining if the load and store access the same address (see co1.5, lines 16-19). The address was referenced or specified by the instruction. Amerson's address was referenced by load and store instructions (col.3, lines 1-10), the referenced address was shown to be the address (e.g. A3) of the load instruction (see col.2, lines 10). The referenced address (e.g. A3) was a value designated by the program as an address operand in the instruction , not by calculation. This address specified by the load instruction was further taught to be compared with the address specified by other store instruction (e.g. see col.8, lines 29-42), and the subsequent action was that upon detection of the match, the data was forwarded to CPU (see col.8, lines 37-42).

22. The referenced address was not being calculated because it was an instruction with the operand address (A3) being designated by the LOAD instruction (see the format of the instruction in see col.l , lines 60-65, col.2, lines 7-15, col.4, lines 43-48c01.6, lines 10-17, col.7, lines 20-26). Amerson did not explicitly characterize his comparison of the load address with store address as "without calculating" the address as claimed. However, by comparing the load and the store addresses to find the same address, the comparison was a logic operation, not a arithmetic operation, therefore , no calculation was being used. Therefore, upon this interpretation, Amerson also did not calculate the address because there was no need for calculating the same address. The subsequent action was that the load instruction in question had a flag set indicating the same address with the store, and the data was forwarded, or loaded (see col.8, lines 37-43). If the address calculation were needed, it would defeat the purpose of address operand comparison (see col.3, lines 31-40 for the data sent to the processor that would have been generated by the load instruction).

23. As to claims 3, 5, 13, 15, Amerson also detected store in a second location that was previously read (loaded, or read by load instruction. See detection of a store accessing the same address with a load in col.5, lines 29-38, col.6, lines 57-66).

24. As to claims 4,14, Amerson also included location previously stored (see col.8, lines 30-41).

25. As to claims 6,7,16,17, Amerson also included symbolic structure (see A3 in load instruction in col.2, line 10).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 20,21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Engebretsen et al. (5,860,138) in view of Ball (5,615,357).

a) detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax for computing an effective address for said first memory location (see the store instruction and the operands needed to compute the effective address in fig.7)',

b) detecting a second instruction that loads data from a second memory location, said second instruction comprising syntax for computing an effective address for said second memory location (see the load instruction format and the operand needed to compute the effective address in fig.3).

27. Engebretsen did not specifically show the determination of syntax relationship between said first memory location and said second memory location, without computing said effective address for said first memory location and without computing said effective address for said second memory location' as clamed. However, Ball

disclosed a system including a determination of syntax relationship (see the model of CPU) without itself calculating effective addresses of the first a and second instructions (see the trace file containing the load and store instruction effective addresses in col.2, lines 39-45, lines 64-67, col.3, lines 1-6, col.4, lines 1-11, col.11, lines 59-67, see col.10, lines 10-52 for the trace driven mode, see col.12, lines 1-7 for load and store). It would have been obvious to one of ordinary skill in the art to use Ball in Engebretsen for including the determination of the syntax without calculating the effective addresses as claimed because the use of Ball could provide Engebretsen the ability to predict the effective address of the instructions (e.g. load and store) based on the performance statistics (e.g. the trace file), therefore by reducing the latency of caused by the effective address calculation during execution cycle , and therefore minimizing the overall time of the processing , and because Engebretsen also taught that if an instruction references a memory location , a data cache can be checked if the referenced memory location is mapped into the data cache, and if it is, there is no need to go to the memory to obtain the data (see col.2, lines 17-25), which was , therefore, a suggestion of the need for not having to calculate the memory address (for example, no need to go to the memory , therefore, no address calculation was needed) in order to increase the processing efficiency, and in doing so, provided a motivation.

28. Claims 8,9, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches

the combined features of the identical offset address value from identical base address in a register within the pipeline microprocessor.

29. Claims 10, 11, 18,19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of instruction decoder stage for detecting load/store data from identical memory location by identifying the offset address from identical base address in a register, and the bypass signal to instruction execution stage that reference to an identical memory location.

30. Amerson (5,475,823) was cited to applicant on the record, therefore, copy is not being provided herein.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Reinman et al., "Predictive Technique for Aggressive Load Speculation", Microarchitecture , 1998, is cited for the teaching of bypassing the calculation of the effective address of load instruction , see Abstract.

b) Johnson et al. (5,761,740) is cited for the teaching of the symbolic structure of the instruction (see fig.7);

c) Riordan (5,606,683) is cited for the teaching of without complete computation of the memory address (see col.2, lines 8-17).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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